UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/016,196	10/30/2001	Hiep P. Ngo	SMQ-067/P5716	4366

959 7590 01/19/2006

LAHIVE & COCKFIELD, LLP.
28 STATE STREET
BOSTON, MA 02109

EXAMINER	
PERILLA, JASON M	

ART UNIT	PAPER NUMBER
2638	

DATE MAILED: 01/19/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Advisory Action Before the Filing of an Appeal Brief	Application No. 10/016,196	Applicant(s) NGO ET AL.	
	Examiner Jason M. Perilla	Art Unit 2638	

--The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

THE REPLY FILED 03 January 2006 FAILS TO PLACE THIS APPLICATION IN CONDITION FOR ALLOWANCE.

1. ☒ The reply was filed after a final rejection, but prior to or on the same day as filing a Notice of Appeal. To avoid abandonment of this application, applicant must timely file one of the following replies: (1) an amendment, affidavit, or other evidence, which places the application in condition for allowance; (2) a Notice of Appeal (with appeal fee) in compliance with 37 CFR 41.31; or (3) a Request for Continued Examination (RCE) in compliance with 37 CFR 1.114. The reply must be filed within one of the following time periods:
   a) ☐ The period for reply expires _____ months from the mailing date of the final rejection.
   b) ☒ The period for reply expires on: (1) the mailing date of this Advisory Action, or (2) the date set forth in the final rejection, whichever is later. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of the final rejection.

   Examiner Note: If box 1 is checked, check either box (a) or (b). ONLY CHECK BOX (b) WHEN THE FIRST REPLY WAS FILED WITHIN TWO MONTHS OF THE FINAL REJECTION. See MPEP 706.07(f).

Extensions of time may be obtained under 37 CFR 1.136(a). The date on which the petition under 37 CFR 1.136(a) and the appropriate extension fee have been filed is the date for purposes of determining the period of extension and the corresponding amount of the fee. The appropriate extension fee under 37 CFR 1.17(a) is calculated from: (1) the expiration date of the shortened statutory period for reply originally set in the final Office action; or (2) as set forth in (b) above, if checked. Any reply received by the Office later than three months after the mailing date of the final rejection, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

NOTICE OF APPEAL

2. ☐ The Notice of Appeal was filed on _____. A brief in compliance with 37 CFR 41.37 must be filed within two months of the date of filing the Notice of Appeal (37 CFR 41.37(a)), or any extension thereof (37 CFR 41.37(e)), to avoid dismissal of the appeal. Since a Notice of Appeal has been filed, any reply must be filed within the time period set forth in 37 CFR 41.37(a).

AMENDMENTS

3. ☐ The proposed amendment(s) filed after a final rejection, but prior to the date of filing a brief, will not be entered because
   (a) ☐ They raise new issues that would require further consideration and/or search (see NOTE below);
   (b) ☐ They raise the issue of new matter (see NOTE below);
   (c) ☐ They are not deemed to place the application in better form for appeal by materially reducing or simplifying the issues for appeal; and/or
   (d) ☐ They present additional claims without canceling a corresponding number of finally rejected claims.

   NOTE: _____. (See 37 CFR 1.116 and 41.33(a)).
4. ☐ The amendments are not in compliance with 37 CFR 1.121. See attached Notice of Non-Compliant Amendment (PTOL-324).
5. ☐ Applicant's reply has overcome the following rejection(s): _____.
6. ☐ Newly proposed or amended claim(s) _____ would be allowable if submitted in a separate, timely filed amendment canceling the non-allowable claim(s).
7. ☐ For purposes of appeal, the proposed amendment(s): a) ☐ will not be entered, or b) ☐ will be entered and an explanation of how the new or amended claims would be rejected is provided below or appended.

   The status of the claim(s) is (or will be) as follows:
   Claim(s) allowed: _____.
   Claim(s) objected to: _____.
   Claim(s) rejected: _____.
   Claim(s) withdrawn from consideration: _____.

AFFIDAVIT OR OTHER EVIDENCE

8. ☐ The affidavit or other evidence filed after a final action, but before or on the date of filing a Notice of Appeal will not be entered because applicant failed to provide a showing of good and sufficient reasons why the affidavit or other evidence is necessary and was not earlier presented. See 37 CFR 1.116(e).
9. ☐ The affidavit or other evidence filed after the date of filing a Notice of Appeal, but prior to the date of filing a brief, will not be entered because the affidavit or other evidence failed to overcome all rejections under appeal and/or appellant fails to provide a showing a good and sufficient reasons why it is necessary and was not earlier presented. See 37 CFR 41.33(d)(1).
10. ☐ The affidavit or other evidence is entered. An explanation of the status of the claims after entry is below or attached.

REQUEST FOR RECONSIDERATION/OTHER

11. ☒ The request for reconsideration has been considered but does NOT place the application in condition for allowance because: See attached response to argument.
12. ☐ Note the attached Information Disclosure Statement(s). (PTO/SB/08 or PTO-1449) Paper No(s). _____
13. ☐ Other: _____.

KENNETH VANDERPUYE
SUPERVISORY PATENT EXAMINER

Response to Arguments

1. Applicant's arguments filed October 10, 2001, see page 10, have been fully considered but they are not persuasive.

2. Regarding the Applicant's arguments against the prior art rejection of claims 1-3, 6-8, 10, 13, and 14 as being anticipated by U.S. Pub. No. 2003/002608 to Glenn et al ("Glenn"), the arguments are not persuasive. The Applicant asserts the following deficiencies in the disclosure of Glenn as applied to the claims of the instant application: (1) Glenn does not disclose a phase locked loop (PLL) as claimed in claim 1, and (2) Glenn does not disclose correcting a timing alignment of a data signal and a clock signal each time said data signal and clock signal are transmitted.

Regarding (1), Glenn's *disclosure of a PLL*, the Applicant suggests that Glenn fails to disclose a phase comparison stage of a PLL and further fails to disclose a voltage controlled oscillator in he PLL. It is noted by the Examiner that a phase comparator is not a claimed component of the PLL and may not be necessary in the broadest interpretation of a PLL. However, to illustrate how Glenn discloses phase locking, the Examiner cites reference 501 of figure 5 as a phase comparison stage of the PLL. Particularly, as shown in the exploded view of the control circuit (fig. 4, ref. 405), reference 501 of figure 5 comprises a phase comparator (para. 0051). It is a phase comparator because it compares the phases of the pre-data, data, and post-data inputs. The Applicant states on page 14, line 3, of the arguments, "Glenn discloses the phase adjust unit compares either the logic values, the running average of the logic values, or the correlation between the patterns . . . and does not compare the relative

phase difference . . . ." The Examiner agrees that the cited phase comparator of Glenn does indeed compare logic values and commands that a comparison of logic values comprises a comparison of phase. Such is consistent with a digital logic phase comparator as notoriously known in the art. A phase comparator of a digital clock signal must necessarily compare logic values because a digital clock signal takes one of two logic states. Further, in relation to clock signals, differing logic states denotes differing phase which may be captured by a phase comparator. Therefore, a comparator that compares logic states is nonetheless a phase comparator.

The Applicant notes that "Glenn does not disclose a voltage controlled oscillator ("VCO") which is a critical component of any PLL." (pg. 14, lines 9-10). The Examiner points out that the claimed phase locked loop (claim 1, line 11) does not explicitly comprise a voltage controlled oscillator, and the claimed phase locked loop will not be presumed to contain one. However, as broadly as claimed, Glenn does disclose a phase locked loop which takes an input from the control circuit and provides it with a phase locking control input as illustrated in figure 4. Furthermore, Glenn discloses in paragraph 0026:

> "The recognition of clock lead or clock lag conditions, as described above, can be used to implement *a stable feedback loop* that continually drives *the phase position 202a of the clock* to be properly *aligned*. That is, once the phase position 202a of the clock is properly aligned, any subsequent "drifting" of the clock towards a lead or lag condition can be identified and used to drive the clock back to its proper position prior to any inaccurate data samplings from the clock."

Therefore, Glenn plainly illustrates and discloses a PLL because a stable feedback ***loop*** is presented which drives the ***phase*** position of the clock into alignment or ***lock***.

Regarding (2), Glenn's *disclosure of correcting a timing alignment of a data signal and a clock signal each time said data signal and clock signal are transmitted*, the Applicant construes the claim language outside that which is the Applicant's own invention. Admittedly, in the narrowest terms as suggested by the Applicant, Glenn's system is not required to correct timing alignment *each and every* time data and clock are transmitted. However, one may infer that it is possible that a timing alignment may be required each time there is a transmission if there is a significant problem with the transmission link (Glenn; para. 0004). Additionally, Glenn does disclose in one embodiment that the phase position of the clock may be permitted to "dither" back and forth which satisfies the claimed correction during every transition (para. 0037). Moreover, Examiner asserts that a correction of a timing alignment for each transmission is not disclosed in the Applicant's own invention. One would not expect that the invention of the instant application provides a "correction" (in a broad sense) each and every time a transmission occurs, and the claim language does not sufficiently distinguish itself from the prior art reference Glenn. While the invention of the instant application may perform or act on the data and clock signals each time a transmission is made, it does not follow that it performs a "correction" each time because, as in the system of Glenn, a correction may not be required each time.

3. Regarding the Applicant's arguments against the prior art rejection of claims 28, 30, and 32 as being anticipated by Glenn, the arguments are not persuasive. The Applicant asserts that the prior art reference Glenn fails to disclose the claimed detection circuit.

The Examiner set forth in the final office action that Glenn discloses the claimed control circuit in reference 405 of figure 5. The Applicant counters the assertion in his arguments on page 16, lines 18-20, by stating "Glenn still fails to disclose a detection circuit for detecting a phase differential between a data signal and a source clock, because Glenn does not use the source clock signal to determine when to make a phase adjustment." Hence, the Applicant is pointing to the fact that Glenn's detection of a phase differential does not rely solely upon a detection of a difference between the data signal and the clock signal directly but rather upon a difference between the data signal, the clock signal, and a phase shifted *copy* of the clock signal.

Specifically, the claimed detection circuit detects "a phase differential between a first data signal . . . and a source clock signal." As broadly as claimed, Glenn discloses that the detection circuit detects a phase differential because it utilizes, collectively, the inputs (fig. 5, "PRE DATA", "DATA", and "POST DATA") which represent a type of "coded" phase differential between the data and clock signals. The Applicant's assertion aside, it is plain from the disclosure of Glenn (and the argument above) that a phase differential between the clock and data signals is detected (para. 0027-0029). Therefore, the detection of the claimed *phase differential* is disclosed by Glenn although, as pointed out by the Applicant, Glenn does not disclose a direct comparison between the data and clock signal phases.